WHAT IS CLAIMED IS:

1. A semiconductor device transmitting/receiving data in a normal mode and refreshing stored data with reduced current consumption in a power down mode, comprising:

a memory array including a plurality of memory cells arranged in a matrix of rows and columns;

a first peripheral circuit inputting/outputting storage data in said memory cells in said normal mode and stopping operation in said power down mode for reducing current consumption; and

a second peripheral circuit controlling refresh of data stored in said memory cells in said power down mode.

2. The semiconductor device according to claim 1, wherein

said second peripheral circuit includes a refresh control unit controlling refresh of a partial region of said memory array by holding a start address indicating an address where the refresh is started and an end address indicating an address where the refresh is ended.

3. The semiconductor device according to claim 2, wherein

said refresh control unit includes:

a timer circuit generating a reference clock for activating a row of said memory array in the refresh; and

an address counter outputting an address for refresh between said start address and said end address,

said address counter includes

a first latch circuit holding said start address,

a second latch circuit holding said end address,

a counter taking count according to said reference clock,

a first comparison circuit comparing an output of said counter with an output of said first latch circuit,

a second comparison circuit comparing the output of said counter with an output of said second latch circuit, and

a gate circuit receiving respective outputs of said first and second comparison circuits to detect that the output of said counter is at least said start address and at most said end address, and

said refresh control unit further includes a delay circuit for control activated according to an output of said gate circuit to output a timing signal for controlling row selection of said memory array according to said reference clock.

4. The semiconductor device according to claim 2, wherein

said refresh control unit includes:

a timer circuit generating a reference clock for activating a row of said memory array in the refresh; and

an address counter outputting an address for refresh between said start address and said end address,

said address counter includes

a first latch circuit holding said start address,

a second latch circuit holding said end address,

a detecting circuit receiving respective outputs of said first and second latch circuits to designate a cycle of said reference clock to said timer circuit according to ratio of a region designated by said start address and said end address to region of said memory array,

a counter receiving the output of said first latch circuit, taking count according to said reference clock using said start address as an initial count, and outputting a refresh address, and

a comparison circuit comparing an output of said counter with the output of said second latch circuit to detect that the refresh is completed.

5. The semiconductor device according to claim 1, further comprising:

a first power supply terminal receiving a first supply potential;

a second power supply terminal receiving a second supply potential higher than said first supply potential;

a first power supply line connecting said first supply terminal and

said first peripheral circuit;

a voltage down converter circuit connected to said second power supply terminal and outputting a third supply potential lower than said second supply potential;

a power supply selection circuit receiving said first power supply potential and said third power supply potential to selectively output one of the received power supply potentials; and

a second power supply line supplying output of said power supply selection circuit to said second peripheral circuit.

6. The semiconductor device according to claim 5, wherein

said power supply selection circuit includes:

a first MOS transistor connected between said first power supply line and said second power supply line and activated in said normal mode; and

a second MOS transistor connected between said voltage down converter circuit and said second power supply line and activated in said power down mode.

7. The semiconductor device according to claim 6, wherein

said power supply selection circuit further includes a voltage converter circuit supplying an activation potential equal to an output potential of said voltage down converter circuit to gate of said second MOS transistor in said power down mode.

8. The semiconductor device according to claim 5, further comprising a logic portion receiving supply potential from said first power supply line and performing a predetermined processing according to an externally supplied instruction, wherein

said first peripheral circuit includes a data input/output control unit for transmitting and receiving data between said logic portion and said memory array,

said second peripheral circuit includes a self refresh control unit

controlling self refresh for said memory array in said power down mode, and

said first power supply terminal receives an inactive potential in said power down mode.

9. The semiconductor device according to claim 8, wherein

said first peripheral circuit further includes:

a clock control unit receiving a clock signal from said logic portion to generate an internal clock signal for transmitting and receiving data to and from said memory array;

a column-related command control unit receiving an instruction from said logic portion to generate a column-related command; and

a column address control unit receiving a column address from said logic portion to select a column of said memory array.

10. The semiconductor device according to claim 9, wherein

said memory array includes a plurality of banks capable of operating independently of each other, and said first peripheral circuit further includes:

a row address control unit receiving a row address from said logic portion to select a row of said memory array; and

a bank address control unit receiving a bank address from said logic portion to select any of said plurality of banks.

11. The semiconductor device according to claim 8, wherein

said memory array includes:

a write data line transmitting write data to said memory cells;

a latch circuit receiving power supply potential from said first power supply line, and receiving and holding data from said data input/output control unit in said normal mode; and

a gate circuit receiving power supply potential from said second power supply line, transmitting an output of said latch circuit to said write data line in said normal mode, and fixing potential of said write data line in said power down mode.

12. The semiconductor device according to claim 8, wherein

said memory array includes:

a read data line for reading data from said memory cells;

a read amplifier circuit receiving power supply potential from said first power supply line, amplifying potential change of said read data line and transmitting the amplified potential change to said input/output control unit in said normal mode; and

a switch circuit coupling said read data line to said second power supply line in said power down mode.

13. The semiconductor device according to claim 8, wherein

said self refresh control unit outputs a refresh address in said power down mode,

said second peripheral circuit further includes an address synthesizing unit receiving a normal address from said logic portion in the normal mode and said refresh address, and

said address synthesizing unit includes:

a first group of MOS transistors connected in series between an internal node and a ground node and each having its gate receiving any of address bits of said normal address;

a second group of MOS transistors connected in series between said internal node and said ground node and each having its gate receiving any of address bits of said refresh address; and

a switch circuit connected between said second power supply line and said internal node and precharging said internal node.

14. The semiconductor device according to claim 13, wherein

said second group of MOS transistors has a greater threshold voltage than that of said first group of MOS transistors.

15. The semiconductor device according to claim 8, wherein

said self refresh control unit outputs a first command signal in the self refresh,

said second peripheral circuit further includes a command synthesizing unit receiving a second command signal supplied from said logic portion in the normal mode and said first command signal, and

said command synthesizing unit includes:

a first P channel MOS transistor connected between said second power supply line and a first internal node and having its gate connected to a second internal node;

a second P channel MOS transistor connected between said second power supply line and said second internal node and having its gate connected to said first internal node;

a first N channel MOS transistor having its gate receiving said first command signal and connected between said second internal node and a ground node;

a second N channel MOS transistor rendered conductive in said self refresh to transmit said first command signal to said first internal node;

a third N channel MOS transistor having its gate receiving said second command signal and connected between said second internal node and said ground node; and

a fourth N channel MOS transistor rendered conductive in said normal mode to transmit said second command signal to said first internal node.

16. The semiconductor device according to claim 15, wherein

said first and second N channel MOS transistors have a greater threshold voltage than that of said third and fourth N channel MOS transistors.

17. The semiconductor device according to claim 8, wherein

said logic portion outputs a mode switch signal indicating transition to said power down mode,

said second peripheral circuit further includes a holding circuit holding mode information indicating said power down mode according to said mode switch signal, and

said holding circuit receives a reset signal from said logic portion when mode returns from said power down mode to said normal mode, and resets said mode information when said holding circuit receives a command signal a predetermined number of times from said logic portion.